Press Release: FIRST STANDARD FOR 3D CHIPS

(July, 2008) The 3D-IC Alliance has produced the first published standard for three-dimensional chip designs: a specification for integrating memory and logic in a 3D stack. This standard lays the cornerstone for memory-to-logic 3D integration and establishes a basis for future collaborative efforts in the industry.

The Intimate Memory Interconnect Standard (IMIS™) defines a high-bandwidth vertical bus implemented on the faces of a memory device and a host device so that, when stacked and bonded, the two devices act as a single integrated circuit. The "intimate" 3D connection treats the memory device like embedded memory with no need for typical chip-to-chip I/O or ESD structures. The face-to-face vertical connections are extremely short, providing fast access and low capacitance.

IMIS™ provides support for multiple data ports with memory busses up to 1,024 bits wide. It addresses several memory device types including SRAM, DRAM, and Flash. The standard includes a system of pin definitions, specifying locations and order, made as generic as possible in order to cover a wide range of implementations. It also contains a set of surface preparation requirements to cover various categories of bonding methods.

This open standard is available on the 3D-IC Alliance website (3D-IC.org) for implementation in any chip design. By providing and promoting open standards the Alliance intends to simplify 3D chip design and allow mainstream adoption of 3D-IC technology. By the end of this year, some industry participants will be sampling IMIS-compliant components.

About the 3D-IC Alliance: The 3D-IC Alliance is a consortium for integrated circuit designers, developers, and manufacturers. Its objective is to promote standards for three-dimensional integrated circuits (3D-ICs) in order to accelerate their availability and acceptance.
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